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09/960,152	09/21/2001	Robert E. Bickel	PD-200007	4264

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,152	BICKEL, ROBERT E.	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: In line 9, "each" should be deleted. Appropriate correction is required.

2. Claim 8 is objected to because of the following informalities: In line 4, "detected" should be "detecting". Appropriate correction is required.

3. Claim 12 is objected to because of the following informalities: In lines 2-3, "said at least three support logic devices" lacks antecedent basis. Appropriate correction is required.

4. Claims 14-18 are objected to because of the following informalities: In lines 1, respectively, "system" should be "circuit". Appropriate correction is required.

5. Claim 19 is objected to because of the following informalities: In line 9, "each" should be deleted. Appropriate correction is required.

6. Claim 19 is objected to because of the following informalities: In line 4, "(CPU)" should be inserted after "unit". Appropriate correction is required.

7. Claim 20 is objected to because of the following informalities: In line 3, "detected" should be "detecting". Appropriate correction is required.

8. Claim 24 is objected to because of the following informalities: In lines 2-3, "said at least three support logic devices" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-3, 6-15 and 18-26 is rejected under 35 U.S.C. 102(e) as being anticipated by Fuchs et al. (6,141,770).

As in claim 1, Fuchs discloses a fault tolerant processing circuit that comprises at least three processor groupings each of said at least three processor groupings having a plurality of processor grouping inputs and a plurality of processor grouping outputs (Figures 1 and 3), a processor system clock coupled to the fault tolerant processing circuit (Abstract), a synchronizing circuit comprising a plurality of output synchronizers, each output synchronizer in operative communication with a corresponding respective processor grouping for synchronizing the output of each processor grouping (Abstract, column 7: lines 1-8, column 10: lines 8-11), a logic circuit in operative communication with said synchronizing circuit (Figures 3 and 6), said logic circuit comprising a fault detection circuit and a fault mask circuit (Figure 3, column 7: lines 24-43, column 9: lines 4-6, column 10: line 28 – column 11: line 14), said logic circuit adapted to compare said plurality of processor group outputs to detect errors in any one of said plurality of processor group outputs (Figure 3, column 10: line 28 - column 11: line 14), and a control logic circuit for resetting each of said at least three processor groups when none of said at least three processor groups is in a majority of said processor groups (Figure 6, Abstract, column 13: lines 1-42), wherein said fault mask circuit is adapted to mask the output of a respective processor grouping associated with a detected error and signal a detected error (column 9: lines 4-6).

As in claim 2, Fuchs discloses wherein said synchronizing circuit further comprises continuously active synchronization signals (i.e., every clock cycle) (Abstract, column 7: lines 1-8).

As in claim 3, Fuchs discloses wherein said synchronizing circuit further comprises periodically active synchronization signals (i.e., every clock cycle is considered periodic) (Abstract, column 7: lines 1-8).

As in clam 6, Fuchs discloses wherein an expected rate of transient faults is tuned by a latent fault scrubbing rate (Figure 4, column 11: lines 35-55).

As in claim 7, Fuchs discloses wherein each of said at least three processor groupings comprises a central processing unit (CPU), having an operating step executed during a clock cycle and operating synchronously with each other CPU, each operating step of each CPU being accomplished in parallel and substantially simultaneously with each of the other at least three CPUs each clock cycle (Figure 3, column 7: lines 1-8), each of said at least three CPUs having a plurality of CPU inputs and a plurality of CPU outputs (Figure 3), and a respective support logic device coupled to said plurality of CPU inputs and said plurality of CPU outputs and having a plurality of support logic device inputs and outputs coupled to said respective CPU (i.e., this is interpreted as the bus interface and system bus components connected to the system bus) (Figure 3).

As in claim 8, Fuchs discloses wherein said logic circuit resets each of said at least three processor groups upon detected a fault and, in response, each of said at least three processor groups restart at a hardware defined operating step (state) (Figure 6, column 11: lines 1-4,

column 16: lines 2-4).

As in claim 9, Fuchs discloses wherein said logic circuit interrupts said at least three processor groups when one of said processor groups has a fault, whereby each of said at least three processor groups without detected faults store state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step (Figure 6, column 13: lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

As in claim 10, Fuchs discloses wherein said logic circuit interrupts said at least three processor groups when a minority of said processor groups has a fault, and wherein each of said at least three processor groups without an error stores state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step (Figure 6, column 13: lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

As in claim 11, Fuchs discloses wherein said logic circuit includes fault control and status registers for storing said state information (Figures 6 and 8, column 15: lines 44-56).

As in claim 12, Fuchs discloses wherein each of said at least three support logic devices includes a memory system (Figure 3).

As in claim 13, Fuchs discloses the system in claim 1 above. Fuchs further discloses that this system can be included in computers aboard spacecraft in orbit (interpreted as satellites) (column 1: lines 15-18). Fuchs further discloses a system bus coupled to each of said plurality of processor group inputs and said fault logic circuit output (Figure 3).

As in claim 14, the Applicant is directed to claim 2 above.

As in claim 15, the Applicant is directed to claim 3 above.

As in claim 18, the Applicant is directed to claim 6 above.

As in claim 19, the Applicant is directed to claim 7 above.

As in claim 20, the Applicant is directed to claim 8 above.

As in claim 21, the Applicant is directed to claim 9 above.

As in claim 22, the Applicant is directed to claim 10 above.

As in claim 23, the Applicant is directed to claim 11 above.

As in claim 24, the Applicant is directed to claim 12 above.

As in claim 25, Fuchs discloses a method of masking the effect of a single event upset in a fault tolerant processing system including at least three processor groups, wherein each processor group includes a CPU, an input, an output, and a support logic device (Figure 3, column 6: lines 42-50), that comprises the steps of monitoring each of said plurality of processor group outputs, detecting an error in one of said processor group outputs by comparing the outputs of each of said at three processor groups against each other (Figure 3, column 10: line 28 – column 11: line 14), classifying each processor group as a majority processor group or minority processor group (Figure 6, column 13: lines 1-42), wherein majority processor groups all having equal value outputs and comprising a majority of all processor groups, and wherein minority processing groups each having an output different than each majority processing group (Figure 6, column 1-42), wherein when any processor group is classified as a minority processor group, storing state information for at least one of said processor groups classified as a majority processor group, simultaneously resetting each of said processor groups to restart at a state defined operating step, and restoring said stored state information to each of said processor groups (Figure 6, column 13: lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

As in claim 26, Fuchs discloses wherein, when no processor group is classified as a majority processor group, simultaneously resetting each of said processor groups and initializing each of said processor groups to restart at a state defined operating step (Figure 6, column 13:

lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchs et al. in view of Hanawa et al. (4,745,302).

As in claim 4, Fuchs discloses the system above. However, Fuchs does not clearly disclose wherein said synchronizing circuit further comprises asynchronous signals. Hanawa discloses an asynchronous signal synchronizing circuit (Abstract).

It would have been obvious to a person skilled in the art at the time the invention was made to include asynchronous signals in the synchronizing circuit taught by Fuchs above. This would have been obvious because Hanawa teaches that in today's technology, external input signals have a different frequency than the internal signals, and in order to provide synchronization, the external signals are handled as asynchronous signals (column 1: lines 8-21). A person skilled in the art would have understood the difference in frequencies of the external and internal signals in today's technology, and would have been led to incorporate a similar system like that of Hanawa in order to provide synchronization.

As in claim 16, the Applicant is directed to claim 4 above.

13. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchs et al. in view of Golshan (6,671,841).

As in claim 5, Fuchs discloses the system above. However, Fuchs does not disclose wherein said synchronizing circuit further comprises logic operative to synchronize a JTAG TCLK with said processor system clock. Golshan discloses that the JTAG standard requires a clock that operates at a different frequency of the internal clock, and thus need to be synchronized with the internal clock to avoid skew problems (Figure 4, column 5: lines 35-50, column 6: lines 27-38).

It would have been obvious to a person skilled in the art at the time the invention was made to include a logic operative to synchronize a JTAG TCLK with said processor system clock into the system taught by Fuchs above. This would have been obvious because Fuchs is not limited form including JTAG circuitry, which is very popular in today's computer processors. A person skilled in the art would have understood that is highly likely that the processors taught by Fuchs does include JTAG circuitry, and if so, would need to make sure that the JTAG signals are synchronized with the internal clock to avoid skew problems, as was taught by Golshan above.

As in claim 17, the Applicant is directed to claim 5 above.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB